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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/724,407	11/26/2003	Raffi Codilian	K35A1248	1053

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EXAMINER	
OLSON, JASON C	

ART UNIT	PAPER NUMBER
2651	

DATE MAILED: 03/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/724,407	CODILIAN ET AL.	
	Examiner	Art Unit	
	Jason C Olson	2651	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13-29* is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/06/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Serrano et al. (US 6,215,608), hereafter, Serrano.

Regarding claim 1, Serrano teaches a microprocessor for executing firmware code (see col. 5, ln. 61-65); and an accelerator circuit for performing operations on the sampled servo data while the microprocessor is executing the firmware code, the accelerator circuit comprising (see col. 5, ln. 55-56) a position error signal (PES) calculator circuit for calculating a PES value based on the sampled servo data (see col. 6, ln. 31-33 and 52-63); and a write unsafe (WUS) estimator responsive to the calculated PES value and to a WUS limit parameter (see col. 6, ln. 64-67; it is interpreted by the examiner that the writer inhibit detector is a write unsafe estimator), the WUS estimator further for signaling the microprocessor (see col. 6, ln,. 67-col. 7, ln. 10) when the calculated PES value exceeds the WUS limit parameter (see col. 8, ln. 28-36).

Regarding claim 2 Serrano teaches a bus for transmitting the WUS limit parameter from the microprocessor to the accelerator circuit (see figure 2, item 232, 217, and the line or bus that runs to the write circuit controlled by the microprocessor).

Regarding claim 3 Serrano teaches the accelerator circuit further comprises a WUS limit register for storing the WUS limit parameter (see col. 6, ln. 67-col. 7, ln. 10; it is interpreted by the examiner that the because the program to control the write inhibit detector is stored in memory, the limit, or threshold value is also stored in memory or a register).

Regarding claim 4 Serrano teaches the accelerator circuit further comprises a PES register for storing the calculated PES value (see col. 7, ln. 48-55).

Regarding claim 5 Serrano teaches the PES value is further based on a parameter stored in a parameter register (see col. 5, ln. 61-col. 6, ln. 6, col. 6, ln. 29-37 and 49-63).

Regarding claim 6 Serrano teaches the servo processing accelerator circuit has a plurality of multipliers that may simultaneously perform parallel calculations (see col. 6, ln. 29-63 and figure 2, items 216 and 226; it is interpreted by the examiner that the amplifier and gain control (AGC) act as multipliers that simultaneously perform calculations while the servo data is being sampled).

Regarding claims 7-9: claims 7-9 have limitations similar to those treated in the above rejection(s), and are met by the references as discussed above. Claim 7 however also recites the following limitations as taught by Serrano: a servo-loop compensator for processing the stream of PES values and generating a stream of control effort values for positioning the transducer head during a track following operation (see col. 6, ln. 59-col. 6, ln. 12 and see figure 2, which depicts the servo loop).

Regarding claims 10-12: claims 10-12 have limitations similar to those treated in the above rejection(s), and are met by the references as discussed above. Claim 10 however also recites the following limitations as taught by Serrano: the servo processing accelerator circuit

including a servo-loop compensator for receiving a stream of PES values based on data read from the sampled servo wedges and generating a stream of control effort values based on the stream of PES values for positioning the transducer head during a track following operation (see col. 4, ln. 37-42 and col. 6, ln. 59-col. 7, ln. 6).

Allowable Subject Matter

Claims 13-29 are allowed. Regarding claim 13, the prior art fails to teach alone or in combination a control system having an accelerator circuit for implementing a first sampled servo controller for periodically adjusting, only during a track-following operation under one or more of a first set of predetermined conditions, the control effort signal based on the distributed position information, and for indicating the occurrence of a predetermined condition within a second set of predetermined conditions to the control system; a second sampled servo controller, separate from the accelerator circuit, for periodically adjusting the control effort signal based on the distributed position information during a track-following operation under one or more of the second set of predetermined conditions. Regarding claim 22, the prior art fails to teach alone or in combination a control system having an accelerator circuit for implementing a first sampled servo controller for periodically adjusting, only during a track-folio wing operation under one or more of a first set of predetermined conditions, the control effort signal based on the distributed position information with a first processing delay; a microprocessor, separate from the accelerator circuit, for implementing a second sampled servo controller using firmware code for periodically adjusting the control effort signal based on the distributed position information, with a second processing delay that is substantially greater than the first processing delay, during an

operation under one or more of a second set of predetermined conditions; wherein the control system selects the first sampled servo controller for adjusting the control effort signal during a track-following operation under one or more of a first set of predetermined conditions, and selects the second sampled servo controller for adjusting the control effort signal during an operation under one or more of a second set of predetermined conditions.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Nishida et al. (US 6,657,805) is cited for controlling the read and write operations of a magnetic disk apparatus. Sakai et al. (US 6,414,809) is cited for a data storage device servo control.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason C Olson whose telephone number is (571)272-7560. The examiner can normally be reached on Monday thru Thursday 7:30-5:30; alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dave Hudspeth can be reached on (571)272-7843. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JCO
March 1, 2005

DAVID HUDSPETH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600